REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

In the Office Action, claims 12, 14, 20-21, 23, 28 and 32 were objected to because of informalities. Claims 1-5, 14-20, 25-31 and 34 were rejected under 35 U.S.C. §102(b) as being anticipated by Ajit, et al. (U.S. Patent No. 6,313,672). Claims 6-8 and 10-13 were rejected under 35 U.S.C. §102(b) as being anticipated by Morris, et al. (U.S. Patent No. 5,926,056). Claim 35 was rejected 35 U.S.C. §103(a) as being unpatentable over Ajit, et al. in view of Chow, et al. (U.S. Patent No. 6,060,906). Claims 9, 21-24, 32-33 and 36 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Examiner is thanked for indicating allowable subject matter.

In this Amendment, claim 26 has been cancelled. Claims 5, 15, 19-21, 23, 28, 32, and 36 have been amended to correct matters of form. Claims 1, 6, 14 and 25 have been amended to clarify the invention.

One defining feature of the present invention, as recited in amended claim 1, is a buffer circuit having a gate-tracking circuit and a pair of stacked transistors where the gate-tracking circuit directly connects to the pair of stacked transistors: "and a gate tracking circuit . . . directly connected to each of the pair of stacked transistors." Similarly, claim 6 recites a buffer circuit containing a tracking circuit that has "a transistor whose gate is directly connected to the [stacked] transistors." Claim 14 likewise recites a buffer circuit "wherein the . . . tracking circuit is directly connected to each of the pair of stacked transistors." Finally, claim 25 recites a

system having "a tracking circuit directly connected to . . .each of the stacked transistors." This feature is fully supported by the specification and Figure 3 of the Application which illustrates transistor 334 connected directly to a source/drain region between stacked transistors 320 and 318. Morris, in contrast, teaches a buffer circuit in which a portion of a circuit that the Examiner characterizes as a gate tracking circuit (transistor 105, resistor 108) is isolated from transistors 111 and 112 by transistor 110. Furthermore, transistor 105 is isolated by both a series of transistors 110 and 111 from stacked transistor 112. Therefore, Morris does not teach the feature of the buffer circuit of the present invention, as recited in amended claim 6, wherein a gate tracking circuit is directly coupled to both transistors of a pair of stacked transistors. Although Ajit discloses a buffer circuit that has a pair of coupled NMOS transistors (M6 and M7 in Figure 5), Ajit fails to disclose a buffer circuit having a tracking circuit that is directly connected to a pair of stacked transistors. Accordingly, Applicants respectfully submit that, amended claims 1, 6, 14 and 25 are patentably distinct from the prior art of record, and upon entry of the present Amendment, will be in allowable condition.

In addition, at least for their dependency on allowable claims, dependent claims 2-5, 7-13, 15-24, and 27-36 are also believed to be in condition for allowance.

In view of the foregoing all of the claims in this case are believed to be in condition for allowance. Should the Examiner have any questions or determine that any further action is desirable to place this application in even better condition for issue, the Examiner is encouraged to telephone applicants' undersigned representative at the number listed below.

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Respectfully submitted,

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